What is claimed is:

1. A method of generating a test pattern for an integrated circuit set in m scan flip-flops (m indicates any natural number) when m outputs from a logical circuit are applied to m output terminals through scan flip-flops and output buffers, comprising:

a first process of counting the number of output buffers, whose output values vary, when said m scan flip-flops output input patterns;

a second process of checking a noise value generated when all output values from the output buffers counted in said first process change;

a third process of selecting the output buffers checked in said first process such that the noise value checked in said second process can be within an allowable noise value; and

a fourth process of outputting as a test pattern a pattern obtained by amending the input pattern such that the output values of the output buffers selected in said third process can change.

2. A method of generating a test pattern for an integrated circuit set in m scan flip-flops (m indicates any natural number) when m outputs from a logical circuit are applied to m output terminals through scan flip-flops and output buffers, and when n (n indicates any natural number) outputs from the logical circuit are applied to m output terminals through the output buffers, comprising:

a first process of counting the number of output buffers, whose output values vary, when said m scan flip-flops output input patterns;

a second process of checking a noise value generated when all output values from the output buffers counted in said first process change, and computing a new noise value by adding to the checked noise value a noise value generated when the n output values from the output buffers change;

a third process of selecting the output buffers checked in said first process such that the noise value checked in said second process can be within an allowable noise value; and

a fourth process of outputting as a test pattern a pattern obtained by amending the input pattern such that the output values of the output buffers selected in said third process can change.

3. The method according to claim 1 or claim 2, wherein said second through fourth processes are repeated on said output buffer not selected in said third process when said fourth process is completed.

4. A method of generating a test pattern for an integrated circuit set in m scan flip-flops (m indicates any natural number) when m outputs from a logical circuit are applied to m output terminals through scan flip-flops and output buffers, comprising:

a first process of grouping said scan flip-flops such that a noise value, generated when all output values from said output buffers belonging to a specific group change, can be within a noise allowable value;

a second process of selecting one group from among groups generated in said first process;

a third process of outputting as a test pattern a pattern in which only an output value of an output buffer belonging to the group selected by said second process changes when said n scan flip-flops output input patterns, and output values of output buffers belonging to groups not selected in said second process remain unchanged; and

a fourth process of repeating said second and third processes on the groups not selected in said second process when said third process is completed.